AMENDMENTS TO THE SPECIFICATION

Page 4, please amend paragraph 2 as follows:

FIG. 4 is an example circuitry of an LVDS driving circuit of FIG. 3 according to the embodiment of the present invention. The differential signal output circuit 20 includes four transistors 21, 22, 23, and 24. The transistor 21 and 23 are PMOS transistors coupled to [[a]] an operational voltage source VDD, and the transistor 22 and 24 are NMOS transistors coupled to the ground. The transistor 23 and 24 are coupled to the first output node and the transistor 21 and 22 are coupled to the second output node of the differential signal output circuit 20. The first and the second output node are for outputting an LVDS differential signal.

Page 6, please amend paragraph 2 (bridging pages 6 and 7) as follows:

FIG. 7 is an example circuitry of the reference current control circuit according to the embodiment of the present invention. The reference current control circuit 50 is for providing the first control voltage V1 and the second control voltage V2 to the transistors 21~24 of the differential signal output circuit 20 to control either PMOS transistor 21 and the NOS transistor 24 or the PMOS transistor 22 and the NOS transistor 23 to operate in the ~~triode~~ saturation region. In this manner, the magnitude of the LVDS differential signal outputted from the differential signal output circuit 20 can be controlled through controlling the magnitude of the first control voltage V1 and the second control voltage V2 provided by the reference current control circuit 50. In FIG. 7, the reference current control circuit 50 includes an operational amplifier 51, a current source 52, a first resistor 53, a second resistor 54, the PMOS transistors 56 and 57, and a NMOS transistor 55. Since the transistors 55, 56, and 57 are manufactured through the same manufacturing process, the μnC_{ox} value of the transistors 55, 56, and 57 are substantially the same. Thus, through controlling the W/L ratio of the transistors 55, 56, and 57 (i.e., $\frac{W_{56}}{L_{56}}:\frac{W_{57}}{L_{57}}:\frac{W_{55}}{L_{55}} = 1:n:m$), the currents across the transistors 55 and 56

can be controlled as I_{ref}/n. Accordingly, the first control voltage V1 and the second control voltage V2 can be determined.